Interactive Tools for Teaching Parallelism Concepts

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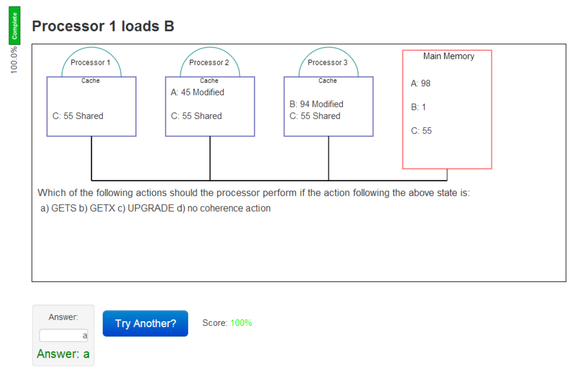
Our work focused on creating sets of interactive problems for the UIUC class ENG 283, Introduction to Parallelism Concepts, that allows students to further their understanding of parallelism. Dr. Craig Zilles developed the project as supplemental material for the class to provide practice and evaluation of learning. In addition to the problems sets we created, which are explained below, others are working on problem sets of various other parallel concepts.

Cache Coherence

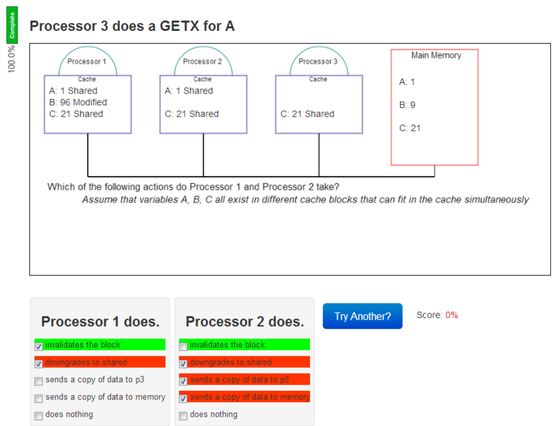
In parallel programing different processors each have their own cache. This lead to the necessity of MSI Protocol (Modified, Shared, Invalid). It's a process to maintain consistent and accurate data in memory.

Processor Actions



This problem evaluates users understanding of one processors request to memory based on the all the processors data states.

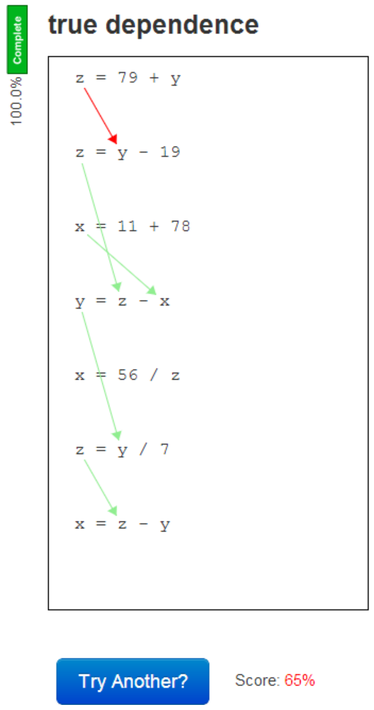
Processor Response



This problem tests users understanding of the interactions of processors when one of the processors make a request on the bus.

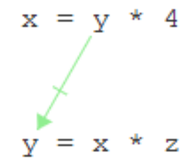
Data Dependencies

There are 3 types of data dependencies, anti, output, and true. These dependencies are problematic because they prevent code from being parallelizable. They also contribute to problems of cache coherency.



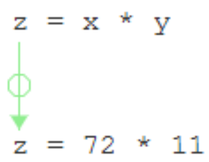
Anti-dependency

An anti-dependency occurs when data is being read then that data is then being written to in a later instruction



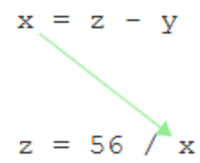
Output dependency

An output dependency occurs when data is being written to then that data is again written to in a later instruction



True dependency

A true dependency (flow dependency) happens when data is being written to then that data is then being read in a later instruction before it is written to again.



Future

Future work on this project could entail developing an interactive problem dealing with data dependencies within MIPS assembly instruction. We are also looking into creating an interactive animation that will aid in visualization of MSI protocol. We will also continue to refine existing problem sets.

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